**JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY KAKINADA**
**KAKINADA – 533 003, Andhra Pradesh, India**

# DEPARTMENT OF CSE - DATA SCIENCE

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| I Year - II Semester | | L | T | P | C |
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| **DIGITAL LOGIC DESIGN (ES1201)** | | | | | |

**Course objectives:**

- To study the basic philosophy underlying the various number systems, negative number representation, binary arithmetic, theory of Boolean algebra and map method for minimization of switching functions.
- To introduce the basic tools for design of combinational and sequential digital logic.
- To learn simple digital circuits in preparation for computer engineering.

**Course outcomes:**

A student who successfully fulfills the course requirements will have demonstrated:

- An ability to define different number systems, binary addition and subtraction, 2's complement representation and operations with this representation.
- An ability to understand the different switching algebra theorems and apply them for logic functions.
- An ability to define the Karnaugh map for a few variables and perform an algorithmic reduction of logic functions.
- Students will be able to design various logic gates starting from simple ordinary gates to complex programmable logic devices & arrays.
- Students will be able to design various sequential circuits starting from flip-flop to registers and counters.

**UNIT I:** Digital Systems and Binary Numbers
Digital Systems, Binary Numbers, Octal and Hexadecimal Numbers, Complements of Numbers, Signed Binary Numbers, Arithmetic addition and subtraction, 4-bit codes: BCD, EXCESS 3, alphanumeric codes, 9's complement, 2421, etc..

**UNIT II:** Concept of Boolean algebra
Basic Theorems and Properties of Boolean algebra, Boolean Functions, Canonical and Standard Forms, Minterms and Maxterms.
Gate level Minimization
Map Method, Three-Variable K-Map, Four Variable K-Maps. Products of Sum Simplification, Sum of Products Simplification, Don't – Care Conditions, NAND and NOR Implementation, ExclusiveOR Function.

**UNIT III:** Combinational Logic
Introduction, Analysis Procedure, Binary Adder–Subtractor, Binary Multiplier, Decoders, Encoders, Multiplexers, Demultiplexers, Priority Encoder, Code Converters, Magnitude Comparator, HDL Models of Combinational Circuits.
Realization of Switching Functions Using PROM, PAL and PLA.

**UNIT IV:** Synchronous Sequential Logic
Introduction to Sequential Circuits, Storage Elements: Latches, Flip-Flops, RS- Latch Using NAND and NOR Gates, Truth Tables. RS, JK, T and D Flip Flops, Truth and Excitation Tables, Conversion of Flip Flops.

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**UNIT V:** Registers and Counters
Registers, Shift Registers, Ripple Counters, Synchronous Counters, Ring Counter, Johnson Counter.

**Text Books:**

1) Digital Design, 5/e, M.Morris Mano, Michael D Ciletti, PEA.
2) Fundamentals of Logic Design, 5/e, Roth, Cengage.

**Reference Books:**

1) Digital Logic and Computer Design, M.Morris Mano, PEA.
2) Digital Logic Design, Leach, Malvino, Saha, TMH.
3) Modern Digital Electronics, R.P. Jain, TMH.